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G4C C11409A

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(54) Fast data transmission circuits for semiconductor memory devices

(57) A data transmission circuit for a semiconductor memory device comprises first and second data transmission lines DB, DBB connected at one end to a first supply voltage and terminating at the other end in first and second sensing nodes N1, N2, means M21, M22 for precharging the data transmission lines to a predetermined voltage level such as ground and for varying the impedance of the data transmission lines in dependence upon signals applied to respective data lines RD, RDB, and means M23, M24 for precharging first and second output nodes N3, N4 to a predetermined voltage level, connecting the output nodes to the respective sensing nodes in response to a transmission pulse PS1 and amplifying M25, M26 a voltage difference between the output nodes by isolating the higher of the output nodes and pulling it up to a second supply voltage Vcc. The first and second output nodes N3, N4 are pulled up via diode connected PMOS transistors M27, M28 to the second supply voltage Vcc. The circuit uses N and P MOS transistors. Additional precharging of the data transmission lines DB, DBB to ground may be provided by NMOS transistors (30, 32 Fig 4).

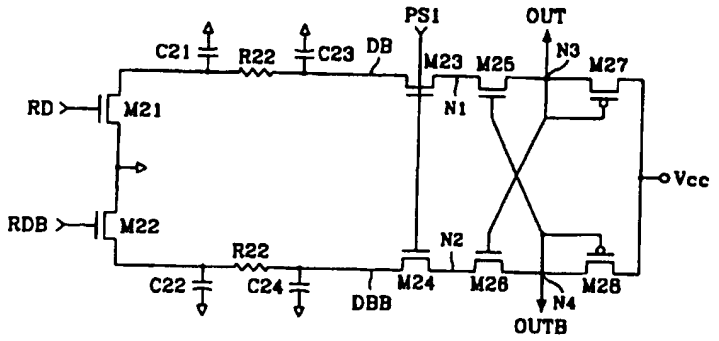

Fig. 2

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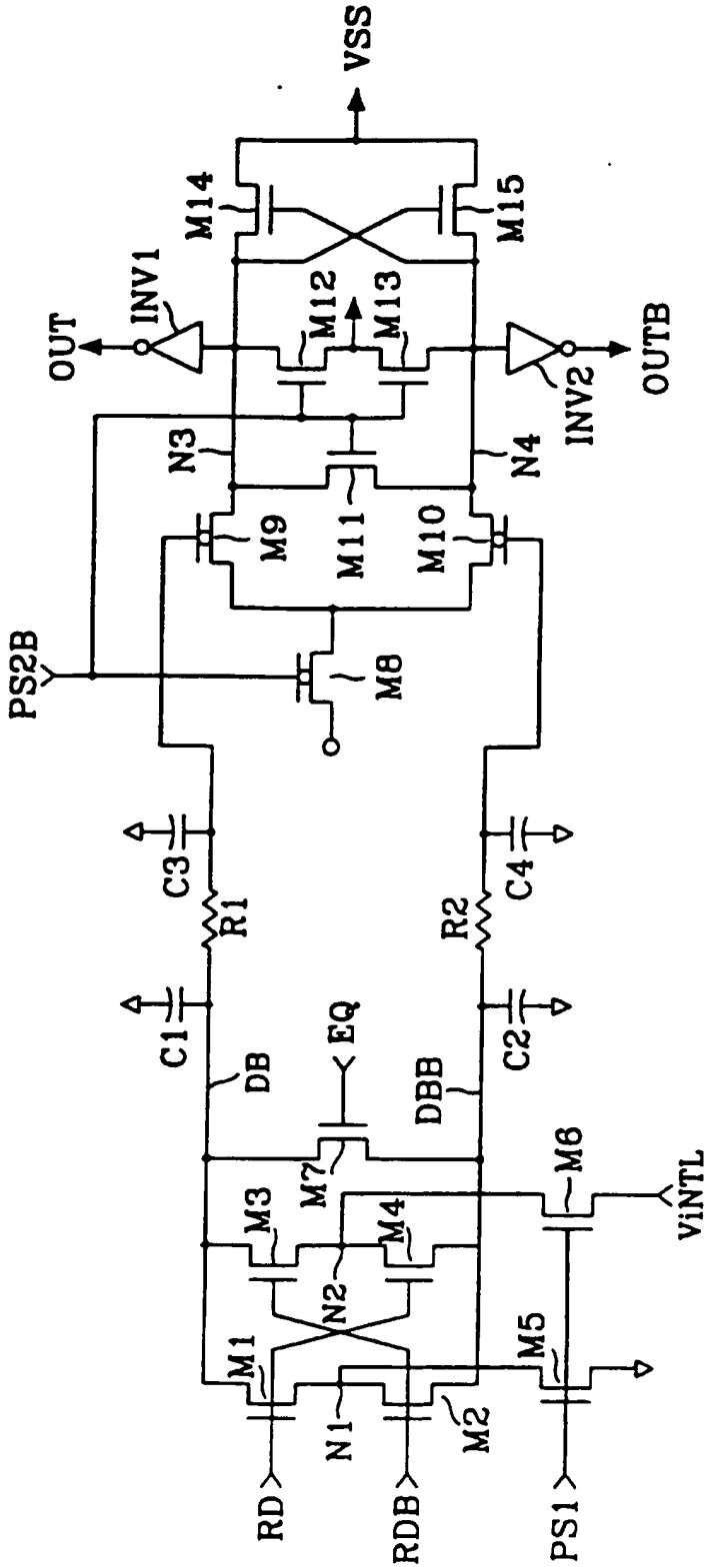

VSS
M14
M15
INV1
OUT
M12
M13
OUTB
INV2
N3
N4
M9
M11
M10
PS2B
M8
C3
C4
R1
R2
C1
C2
EQ
DB
DBB
M7
M6
M3
M4
ViNTL
N2
M1
M5
N1
M2
RD
RDB
PS1

Fig. 1

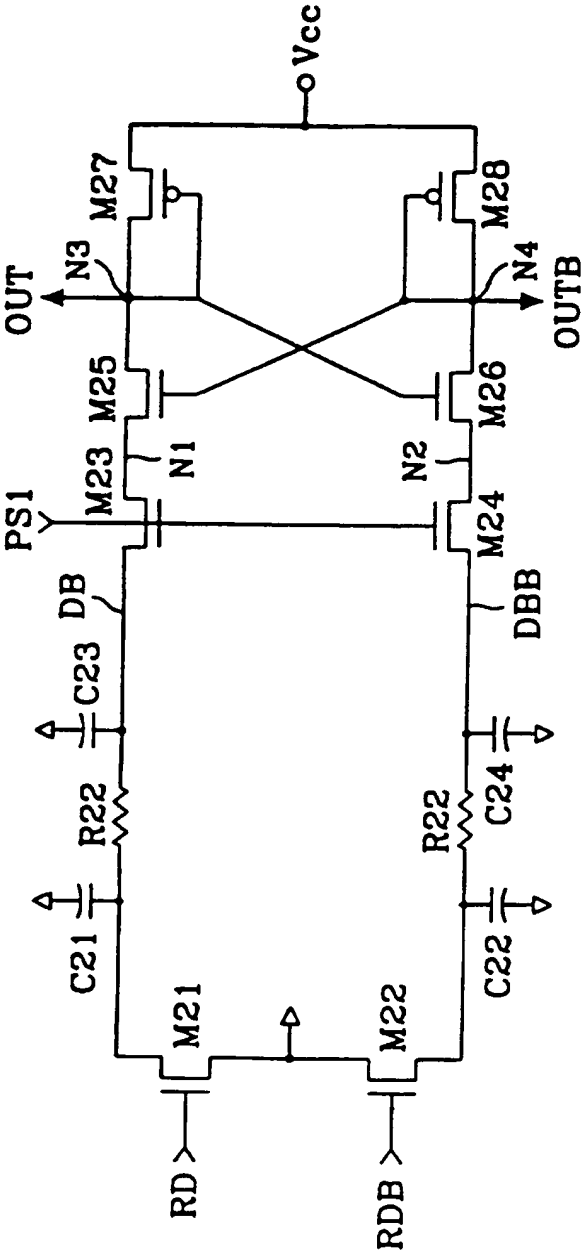
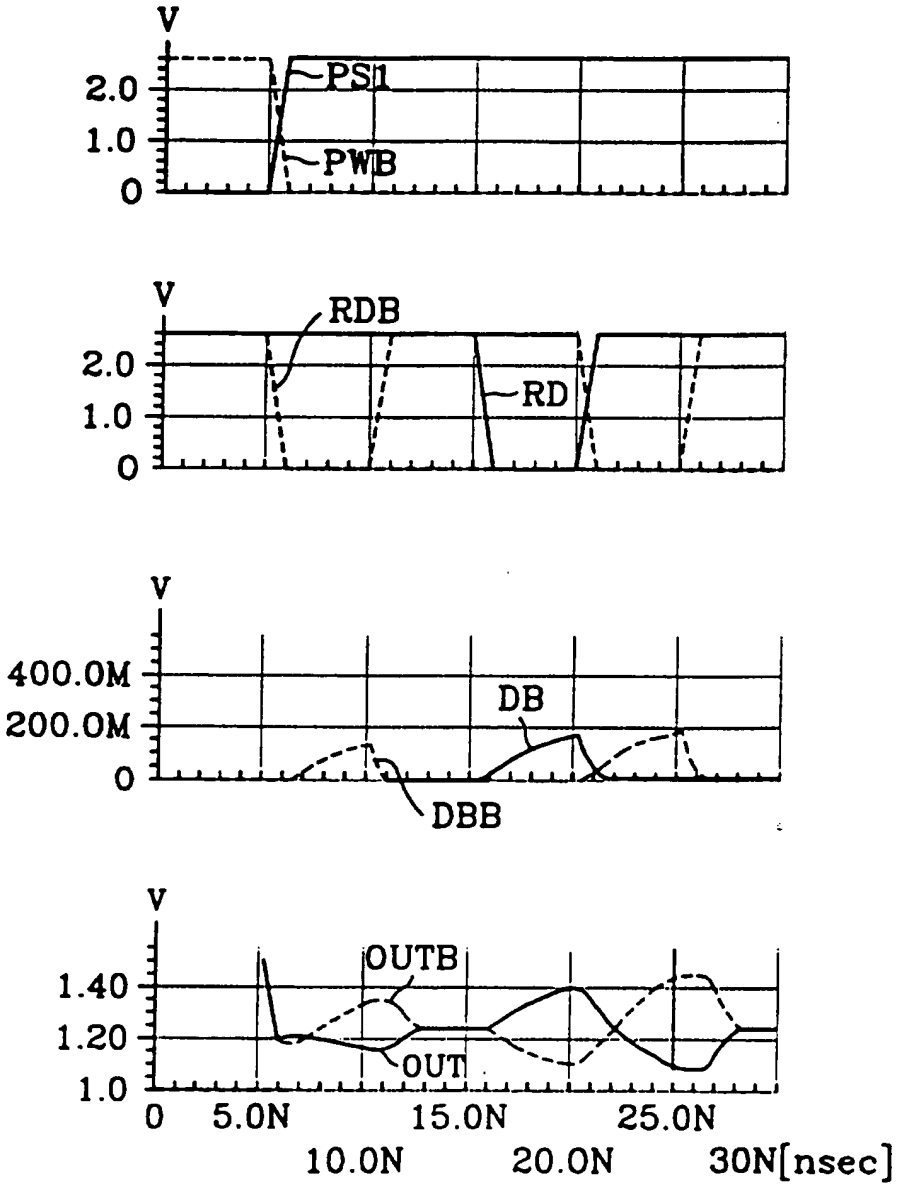

Vcc
M27
M28
OUT
N3
N4
OUTB
M25
M26
N1
N2
PS1
M23
M24
DB
DBB
C23
C24
R22
R22
C21
C22
M21
M22
RD
RDB

Fig. 2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1.0
0
PS1
PWB
V
RDB
RD
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1.0
0
V
400.0M
200.0M
0
DB
DBB
V
OUTB
OUT
1.40
1.20
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0
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10.0N
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Fig. 3

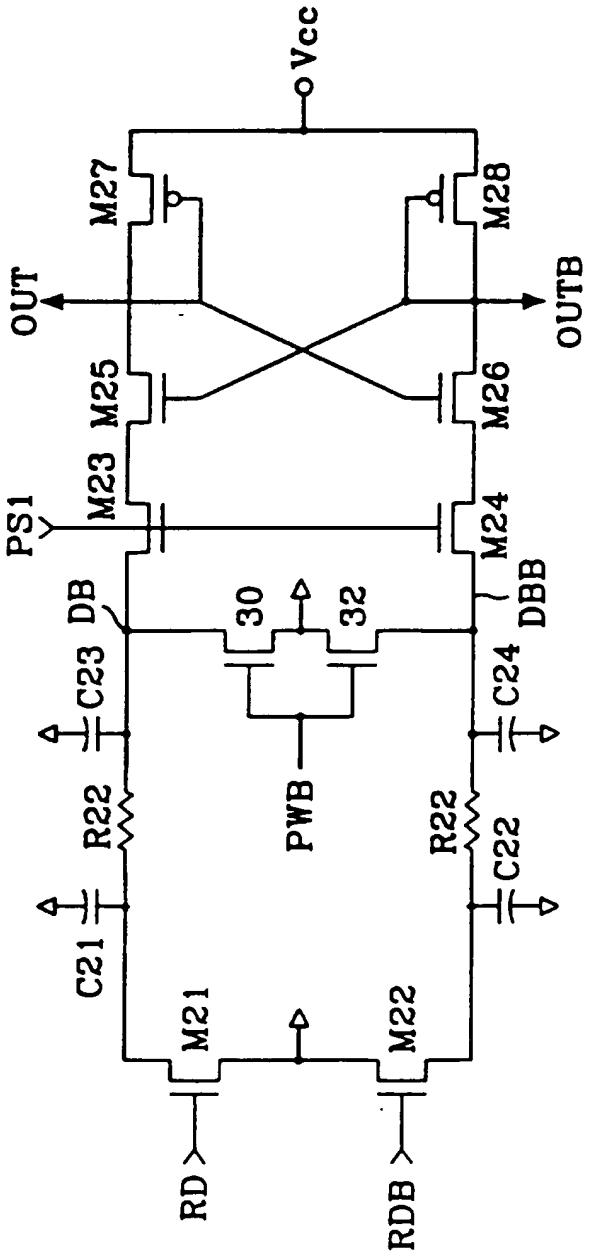
Vcc
M27
M28
OUT
OUTB
M25
M26
M23
PS1
M24
DB
DBB
30
32
C23
C24
R22
PWB
R22
C22
C21
M21
M22
RD
RDB

Fig. 4

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FAST DATA TRANSMISSION CIRCUITS FOR SEMICONDUCTOR MEMORY DEVICES

Background to of the Invention

The present invention relates to data transmission circuits for semiconductor memory devices.

With current advances, higher density and higher capacity integrated semiconductor memory devices are being produced. However, as the density and capacity of the integrated circuit continue to increase, it becomes more important to reduce the operating power of the semiconductor memory device. The usual method of minimizing power consumption is to minimize the current consumed by data transmission lines, as described in an article published by Hisakazu Kotani et. al., in ISSCC 1994, pp 142-143, entitled "A 256Mb DRAM with 100MHZ Serial I/O Ports for Storage of Moving Pictures". This employed a suppressed high differential transfer SHF circuit and will briefly be described with reference to FIG. 1.

Referring to FIG. 1, when a pair of data terminals of a data driver 10 or a data line pair RD/RDB, e.g. the sensing bit line pair of a sense amplifier, have been precharged to a logic "high" state, an equalizing signal is applied in the logic "high" state. Accordingly, the data transmission lines DB/DBB are initially put into an equalized state by an NMOS transistor M7 being turned on. In this equalized state, if the potential of either data line RD or RDB and the equalizing signal EQ change to a logic "low" level, and if a transmission pulse PS1 goes from a logic "low" state to a logic "high" state, the potential of a connection node N1, a common source for NMOS transistors M1 and M2 whose drains are connected to the data transmission lines DB and DBB, is discharged to the first supply voltage level, i.e. ground potential Vss, through the channel of an NMOS transistor M5. At this time, the potential of a connection node N2, a common source for NMOS transistors M3 and M4

whose drains are connected to each of data transmission lines DB and DBB, is developed to the level of the internal supply voltage VINTL supplied through a channel of an NMOS transistor M6.

Assuming that one data line RDB has been changed to the logic "low" state (the other data line RD is provided with a complementary data signal and is maintained in the logic "high" level), NMOS transistors M1 and M4 whose gates are connected to data line RD are turned on, and NMOS transistors M2 and M3 whose gates are connected to the data line RDB are turned off. Accordingly, the level of the data transmission line DB changes to ground potential Vss as NMOS transistors M1 and M3 are turned on and turned off, respectively, and the level of the data line DBB is developed to the level of the internal supply voltage VINTL as NMOS transistors M2 and M4 are turned off and on, respectively.

If a control pulse PS2B for receiving data transmitted to the data transmission line pair DB/DBB is changed from a logic "high" state to a logic "low" state, thus operating a data reception terminal 12, a PMOS transistor M8 whose source is connected to a second supply voltage, i.e. supply voltage Vcc, is turned on. As the PMOS transistor M8 is turned on, PMOS transistors M9 and M10 whose gates are respectively connected to the data transmission lines DB and DBB are supplied with the supply voltage Vcc at their sources. At this time, the levels of the potentials applied to gates of PMOS transistors M9 and M10 are different and therefore, PMOS transistors M9 and M10 have channel conductances different from each other. In such a condition, the potential level of the data transmission line DB is lower than that of the data transmission line DBB and therefore, the channel conductance of the PMOS transistor M9 becomes higher than that of the PMOS transistor M10. Accordingly, voltages of nodes N3 and N4 for drains of PMOS transistors M9 and M10 are respectively developed to the internal supply voltage level VINTL and to

the ground potential Vss level.

If the output node N3 is pulled up to the logic "high" state, the NMOS transistor M15 is turned on and thus, the level of the node N4 is pulled down to the level of the ground potential Vss. Therefore, if the transmission pulse PS2B for receiving data is changed from the logic "high" state to the logic "low" state, the outputs of inverters INV1 and INV2 may be pulled up to the logic "high" state and pulled down to the logic "low" state, respectively, or vice versa. In the configuration shown in FIG. 1, when the control pulse PS2B for receiving data is in the logic "high" state, NMOS transistors M11, M12 and M13 are respectively turned on to precharge nodes N3 and N4 to the level of the ground potential Vss, and perform an equalizing operation.

On the other hand, since the conventional data transmission circuit having the configuration shown in FIG. 1 generates internal supply voltage VINTL only for the data transmission line to narrow the voltage variation of the data transmission line pair DB/DBB, it is very difficult to reduce chip area and also there is the problem that the line for the internal supply voltage VINTL has to be distributed throughout the chip.

Accordingly, it is an object of the present invention to provide a semiconductor memory device capable of reducing power consumption of a data transmission circuit by minimizing voltage variation of data transmission line without the use of data transmission voltage.

It is another object of the present invention to provide a data transmission circuit capable of transmitting data in a low voltage level at a high speed.

Summary of the Invention

Accordingly, the present invention provides a data transmission circuit for a semiconductor memory device

comprising:

first and second data lines;

first and second data transmission lines connected at one end to a first supply voltage and terminating at the other in first and second sensing nodes respectively;

means for precharging the data transmission lines to a predetermined voltage level and for varying the impedance of the data transmission lines in dependence upon the signals applied to respective data lines;

first and second output nodes;

means for precharging the first and second output nodes to a predetermined voltage level, connecting the output nodes to respective sensing nodes in response to a transmission pulse signal and amplifying a voltage difference between the output nodes by shielding the higher voltage output node from its respective sensing node and pulling it up to a second supply voltage level.

Preferably, the means for amplifying a voltage difference between the output nodes comprises a pair of MOS transistors having channels connected between respective output and sensing nodes and control terminals connected to opposite output nodes.

Preferably, the means for varying the impedance of the data transmission lines comprises a pair of MOS transistors having channels connected between respective transmission lines and the first supply voltage and control terminals connected to respective data lines.

Preferably, the means for connecting the output nodes to respective sensing nodes in response to a transmission pulse signal comprises a pair of MOS transistors having channels connected between respective data transmission lines and sensing nodes and control terminals receiving the said transmission pulse signal.

Preferably, the circuit comprises means for pulling up the first and second output nodes to the said second supply

voltage level. The means for pulling up the output nodes may comprise a pair of MOS transistors which are diode-connected between respective output nodes and the second supply voltage.

Preferably, the first supply voltage is ground potential and the second supply voltage is power supply voltage.

The means for precharging the data transmission lines may be adapted so to do in response to a control pulse. For example, such means may comprise a pair of MOS transistors having channels connected between the first supply voltage and respective data transmission lines and control terminals receiving the control pulse.

The present invention also extends to a semiconductor memory device including a data transmission circuit according to the invention.

Brief Description of the Drawings

The present invention will now be described by way of example with reference to the accompanying drawings in which:

Fig. 1 is a circuit diagram illustrating a data transmission circuit used for a conventional memory device;

Fig. 2 is a circuit diagram illustrating a data transmission circuit for a semiconductor memory device according to the present invention;

Fig. 3 is a operation timing diagram explaining the data transmission operation according to the present invention; and

Fig. 4 is a circuit diagram illustrating a data transmission circuit for a semiconductor memory device in accordance with a second embodiment of the present invention.

Detailed Description of the Preferred Embodiments

FIG. 2 illustrates a circuit diagram of a data transmission circuit for a semiconductor memory device, which is

constructed so as to transmit data from a pair of data terminals RD/RDB or data line pairs RD/RDB in response to an input of one control pulse without the use of an additional transmission voltage.

As can be seen in FIG. 3, if both data lines RD and RDB of a data driver are input in a stand-by mode of a logic "high" state, these signals of the logic "high" state are supplied to the gates of NMOS transistors M21 and M22. The drains of NMOS transistors M21 and M22 are connected to respective data transmission lines DB and DBB and their sources are connected in common to a first supply voltage, i.e. ground potential Vss. Accordingly, if a signal of the logic "high" state is input to both of the data lines RD and RDB, NMOS transistors M21 and M22 are turned on and thus, the levels of the data transmission line pair DB/DBB are all precharged to the ground potential Vss level as shown in FIG. 3.

In this stand-by state, a transmission pulse PS1 is input in a second logic state, i.e. in the logic low" state as shown in FIG. 3. If the transmission pulse PS1 is input in the logic "low" state, NMOS transistors M23 and M24 which are respectively connected to data transmission lines DB and DBB are all turned off. At this time, the drain nodes of NMOS transistors M23 and M24, i.e. first and second sensing nodes N1 and N2, are precharged to a half of the supply voltage Vcc level. In detail, if a second supply voltage, i.e. supply voltage Vcc, is supplied to a circuit as shown in FIG. 2, PMOS transistors M27 and M28 which are diode-connected between supply voltage Vcc and output nodes N3 and N4 are turned on. Thus, the levels of the output nodes N3 and N4 are precharged to the voltage Vcc-Vtp level (herein, Vtp is referred to as the threshold voltage of PMOS transistors M27 and M28) as can be seen in FIG. 3, and NMOS transistors M25 and M26 whose gates are respectively connected to output nodes N3 an N4 are turned on, thereby maintaining first and second sensing nodes N1 an N2 in a state precharged to the level of the "Vcc-Vtp-Vtn".

In this stand-by state, if either one of the data lines RD and RDB is changed from the logic "high" state to the logic "low" state, for example, if the data line RDB goes to the logic "low" level as shown in FIG. 3, the NMOS transistor M21 is turned-on and the NMOS transistor M22 is turned off. In such a state, the transmission pulse PS1 is changed from the logic "low" state to the logic "high" state as shown in FIG. 3, NMOS transistors M23 and M24 are turned on in response to the transmission pulse PS1 of the logic "high" state. If the NMOS transistors M23 and M24 are turned on, the first and second sensing nodes N1 and N2 are connected to the respective first and second data transmission lines DB and DBB of the data transmission line pair DB/DBB. As a result, if the transmission pulse PS1 is changed from the logic "low" state to the logic "high" state, supply voltage Vcc flows into the respective data transmission line DB and DBB through a source-drain channel of the first and second PMOS transistors M23 and M24.

Thus, the first NMOS transistor M21 connected to the data transmission line pair DB/DBB is turned on and the second NMOS transistor M22 is turned off. Therefore, the potential of the respective data transmission lines DB and DBB is changed after electrical current flows via NMOS transistors M23 and M24 after a given time period has lapsed. That is, a given potential difference occurs between data transmissions DB and DBB. For example, the potential of the data transmission line DB is discharged to the ground potential Vss level through a drain-source channel of the turned-on NMOS transistor M21, and thus it is pulled-down to the ground potential Vss level as shown in FIG. 3, and the data transmission line DBB has a given potential level which is determined by the amount of charge which has flowed through the second NMOS transistor M24, its capacitances C22 and C24 and its line resistance R2 as shown in FIG. 3.

If the potential of the data transmission lines pair DB/DBB is changed as shown in FIG. 3 as the transmission pulse PS1

is enabled to the logic "high" state, a difference in the channel conductance of the NMOS transistors M23 and M24 occurs and this results in the potential of the first and second sensing nodes N1 and N2 being changed. In other words, the level of the drain of the NMOS transistor M23 is pulled down to the logic "low" state by a data transmission line precharged to the ground potential Vss level and the level of the drain of the NMOS transistor M24 is maintained at the level of the voltage "Vcc-Vtp-Vtn" by the data transmission line DBB which has a given potential level as the NMOS transistor M22 is turned off.

If the level of the first sensing node N1 is pulled down as stated above, the potential of the first output node N3 to which the drain of the NMOS transistor M25 is connected is pulled down to the logic "low" level and the NMOS transistor M26 whose control electrode is connected to the first output node N3 is turned off. Accordingly, the second output node N4 is maintained in the logic "high" state by the PMOS transistor M28 which is diode-connected between the supply voltage Vcc and the second output node N4, thus matching the signal input state of the data line pair RD/RDB to change their output state as shown in FIG. 3 and transmit the signal.

Accordingly, the data transmission circuit having the configuration as shown in FIG. 2 can transmit data without a use of additional data transmission voltage. As in the foregoing example, when the data line RDB of the data line pair RD/RDB is changed from the logic "high" state to the logic "low" state, the levels of the output nodes N22 and N23 are generated through the same procedure as above.

FIG. 4 illustrates a data transmission circuit of the semiconductor memory device in accordance with the second embodiment of the present invention, which additionally includes a circuit for precharging the data transmission line pair DB/DBB shown in FIG. 2 to the ground potential Vss. In FIG. 2, to precharge the first and second data

transmission lines DB and DBB to the ground voltage Vss level, both data and complementary data which are received by the data line pair RD/RDB should be input in the logic "high" state so that NMOS transistors M21 and M22 can be turned on. Therefore, the inventive data transmission circuit having the configuration shown in FIG. 4 aims to resolve such limitations.

The precharge circuit additionally connected between the data transmission lines DB and DBB comprises of two NMOS transistors 30 and 32 whose sources are respectively connected to the ground potential Vss, whose drains are respectively connected to the first and second data transmission lines DB and DBB and whose gates receive a precharge pulse PWB.

The data transmission circuit of FIG. 4 operates in the same manner as the circuit shown in FIG. 2, and performs an additional operation for precharging the data transmission line pair DB/DBB to the ground potential Vss level when the precharge control pulse PWB is input in the logic "high" state. This precharge control pulse PWB has a phase opposite to that of the aforesaid transmission pulse PS1 as can be seen in the timing diagram shown in FIG. 3.

As is apparent from the foregoing, the present invention can reduce the power consumed by the data transmission line by minimizing the voltage variation of the data line without using any additional power supply for transmitting data and ban also efficiently obtain high integration of the device by reducing the size of the data transmission circuit.

CLAIMS:

1. A data transmission circuit for a semiconductor memory device comprising:

first and second data lines;

first and second data transmission lines connected at one end to a first supply voltage and terminating at the other in first and second sensing nodes respectively;

means for precharging the data transmission lines to a predetermined voltage level and for varying the impedance of the data transmission lines in dependence upon the signals applied to respective data lines;

first and second output nodes;

means for precharging the first and second output nodes to a predetermined voltage level, connecting the output nodes to respective sensing nodes in response to a transmission pulse signal and amplifying a voltage difference between the output nodes by shielding the higher voltage output node from its respective sensing node and pulling it up to a second supply voltage level.

2. A circuit according to claim 1 in which the means for amplifying a voltage difference between the output nodes comprises a pair of MOS transistors having channels connected between respective output and sensing nodes and control terminals connected to opposite output nodes.

3. A circuit according to claim 1 or claim 2 in which the means for varying the impedance of the data transmission lines comprises a pair of MOS transistors having channels connected between respective transmission lines and the first supply voltage and control terminals connected to respective data lines.

4. A circuit according to any preceding claim in which the means for connecting the output nodes to respective sensing nodes in response to a transmission pulse signal comprises a pair of MOS transistors having channels connected between respective data transmission lines and

sensing nodes and control terminals receiving the said transmission pulse signal.

4. A circuit according to any preceding claim comprising means for pulling up the first and second output nodes to the said second supply voltage level.

5. A circuit according to claim 4 in which the means for pulling up the output nodes comprises a pair of MOS transistors which are diode-connected between respective output nodes and the second supply voltage.

6. A circuit according to any preceding claim in which the first supply voltage is ground potential and the second supply voltage is power supply voltage.

7. A circuit according to any preceding claim in which the means for precharging the data transmission lines are adapted so to do in response to a control pulse.

8. A circuit according to claim 7 in which the means for precharging the data transmission lines comprises a pair of MOS transistors having channels connected between the first supply voltage and respective data transmission lines and control terminals receiving the control pulse.

9. A data transmission circuit for a semiconductor memory device substantially as described herein with reference to FIGs. 2 or 4 of the accompanying drawings.

10. A semiconductor memory device including a data transmission circuit according to any preceding claim.

The Patent Office

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Application No: GB 9620676.8
Claims searched: 1-10

Examiner: Brian Ede
Date of search: 3 December 1996

Patents Act 1977
Search Report under Section 17

Databases searched:

UK Patent Office collections, including GB, EP, WO & US patent specifications, in:

UK Cl (Ed.O): G4C(C700B, C700C, C706, C11409A, C11409C)

Int Cl (Ed.6): G11C 7/00 7/06 11/409

Other: Online: WPI

Documents considered to be relevant:

Category	Identity of document and relevant passage		Relevant to claims
P A	GB 2289781 A	(HYUNDAI) see Figure 4	1
A	EP 0398245 A2	(KK TOSHIBA) see PR, PA, NA, and CT2 Figure 1	1
A	US 4736343	(MITSUBISHI) see QPR0, QPR1, SA0 and AP0 Figure 3	1

X	Document indicating lack of novelty or inventive step	A	Document indicating technological background and/or state of the art.
Y	Document indicating lack of inventive step if combined with one or more other documents of same category.	P	Document published on or after the declared priority date but before the filing date of this invention.
&	Member of the same patent family	E	Patent document published on or after, but with priority date earlier than, the filing date of this application.